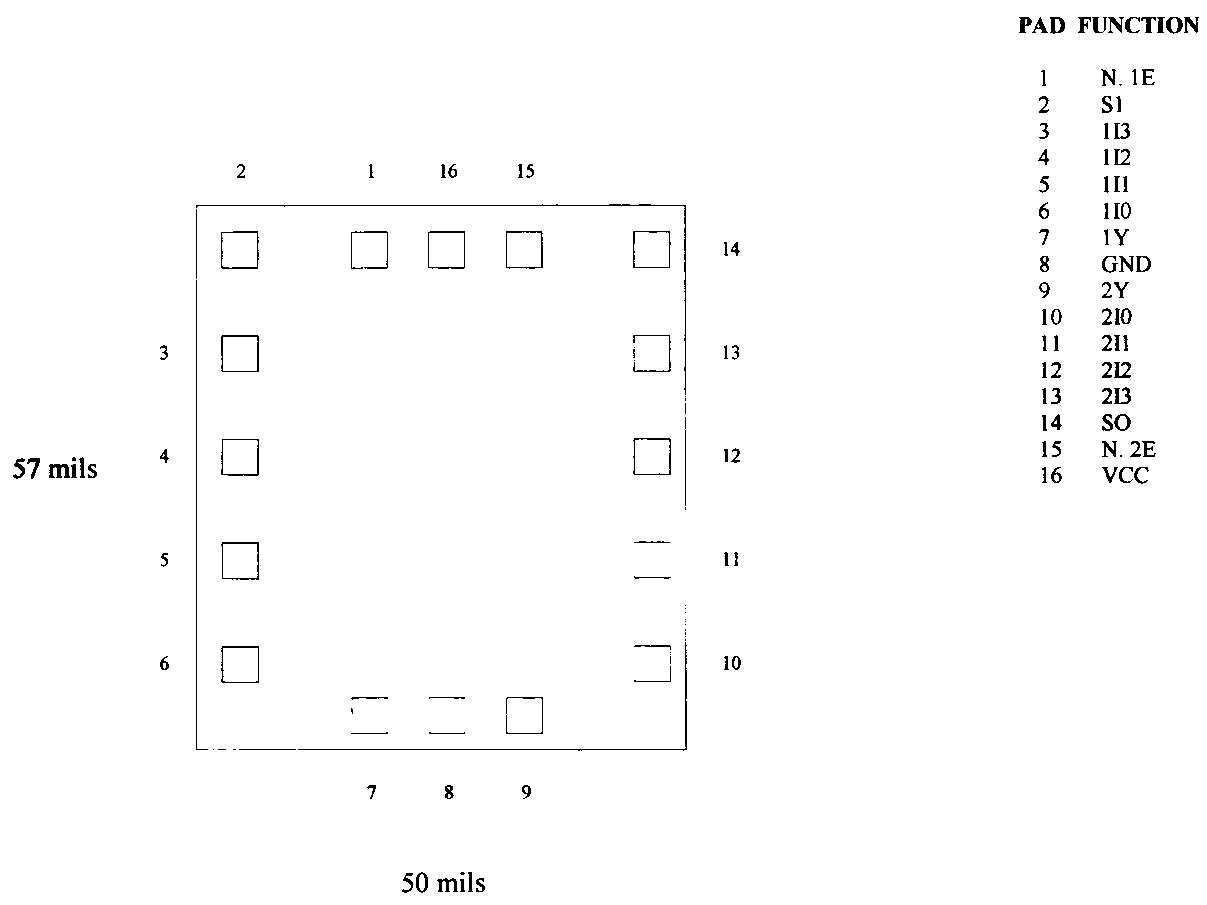
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**PAD FUNCTION:**

1. **N. 1E**
2. **S1**
3. **1I3**
4. **1I2**
5. **1I1**
6. **1I0**
7. **1Y**
8. **GND**
9. **2Y**
10. **2I0**
11. **2I1**
12. **2I2**
13. **2I3**
14. **SO**
15. **N.2E**
16. **VCC**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: ISOLATED**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .050” X .057” DATE: 7/11/22**

**MFG: HARRIS / RCA THICKNESS .014” P/N: 54HC153**

**DG 10.1.2**

#### Rev B, 7/19/02